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High Speed PCB Design - Lee W. Ritchey 1996

High-Speed Signaling - Kyung Suk (Dan) Oh 2011-10-07

New System-Level Techniques for Optimizing Signal/Power Integrity in High-Speed Interfaces--from Pioneering Innovators at Rambus, Stanford, Berkeley, and MIT As data communication rates accelerate well into the multi-gigahertz range, ensuring signal integrity both on- and off-chip has become crucial. Signal integrity can no longer be addressed solely through improvements in package or board-level design: Diverse engineering teams must work together closely from the earliest design stages to identify the best system-level solutions. In High-Speed Signaling, several of the field's most respected practitioners and researchers introduce cutting-edge modeling, simulation, and optimization techniques for meeting this challenge. Edited by pioneering experts Drs. Dan Oh and Chuck Yuan, these contributors explain why noise and jitter are no longer separable, demonstrate how to model their increasingly complex interactions, and thoroughly introduce a new simulation methodology for predicting link-level performance with unprecedented accuracy. The authors address signal integrity from architecture through high-volume production, thoroughly discussing design, implementation, and verification. Coverage includes New advances in passive-channel modeling, power-supply noise and jitter modeling, and system margin prediction Methodologies for balancing system voltage and timing budgets to improve system robustness in high-volume manufacturing Practical, stable formulae for converting key network parameters Improved solutions for difficult problems in the broadband modeling of interconnects Equalization techniques for optimizing channel performance Important new insights into the relationships between jitter and clocking topologies New on-chip measurement techniques for in-situ link performance testing Trends and future directions in signal integrity engineering High-Speed Signaling thoroughly introduces new techniques pioneered at Rambus and other leading high-tech companies and universities: approaches that have never before been presented with this much practical detail. It will be invaluable to everyone concerned with signal integrity, including signal and power integrity engineers, high-speed I/O circuit designers, and system-level board design engineers.

Nanometer CMOS ICs - Harry J.M. Veendrick 2017-04-28

This textbook provides a comprehensive, fully-updated introduction to the essentials of nanometer CMOS integrated circuits. It includes aspects of scaling to even beyond 12nm CMOS technologies and designs. It clearly describes the fundamental CMOS operating principles and presents substantial insight into the various aspects of design implementation and application. Coverage includes all associated disciplines of nanometer CMOS ICs, including physics, lithography, technology, design, memories, VLSI, power consumption, variability, reliability and signal integrity, testing, yield, failure analysis, packaging, scaling trends and road blocks. The text is based upon in-house Philips, NXP Semiconductors, Applied Materials, ASML, IMEC, ST-Ericsson, TSMC, etc., courseware, which, to date, has been completed by more than 4500 engineers working in a large variety of related disciplines: architecture, design, test, fabrication process, packaging, failure analysis and software.

More-than-Moore 2.5D and 3D SiP Integration - Riko Radojicic 2017-02-08

This book presents a realistic and a holistic review of the microelectronic and semiconductor technology options in the post Moore's Law regime. Technical tradeoffs, from architecture down to manufacturing processes, associated with the 2.5D and 3D integration technologies, as well as the business and product management considerations encountered when faced by disruptive technology options, are presented. Coverage includes a discussion of Integrated Device Manufacturer (IDM) vs Fabless, vs

Foundry, and Outsourced Assembly and Test (OSAT) barriers to implementation of disruptive technology options. This book is a must-read for any IC product team that is considering getting off the Moore's Law track, and leveraging some of the More-than-Moore technology options for their next microelectronic product.

OFDM Wireless LANs - John Terry 2002

Annotation Deploy and optimize your wireless LAN using the new standard for broadband wireless communication, OFDM. A comprehensive reference written by two experts who helped create the OFDM specifications. A detailed, practical guide to OFDM WLANs does not exist, requiring readers to seek out multiple sources of information, such as white papers and research notes. Detailed explanations of the concepts and algorithms behind OFDM-context that is missing from the two OFDM books currently available. This book explains OFDM WLAN basics, including components of OFDM and multicarrier WLAN standards. It provides a practical approach to OFDM by including software and hardware examples and detailed implementation explanations. OFDM Multicarrier Wireless Networks: A Practical Approach defines and explains the mathematical concepts behind OFDM necessary for successful OFDM WLAN implementations. Juha Heiskala is a research engineer at Nokia Research Center in Irving, TX. Heiskala is active in the IEEE 802.11 standards bodies and has been tasked with developing the 802.11a system simulation on several software platforms. He is the inventor/co-inventor of three pending patents in the area of OFDM LANs and co-designed with Dr. John Terry the modulation and coding scheme for achieving 100 Mbps speeds within currently allocated band specifications for OFDM WLANs. John Terry, Ph.D. is a senior research engineer at Nokia Research Center. He is currently managing the OFDM modulation and coding project in the HSA group. Dr. Terry has published several white papers, given numerous presentations on wireless communications, and generated four patents related to OFDM WLANs. He has 10 years of experience working in wireless communications, including tenures at NASA Glen Research Center and Texas Instruments.

Digital Signal Processing: World Class Designs - Kenton Williston 2009-03-18

All the design and development inspiration and direction an digital engineer needs in one blockbuster book! Kenton Williston, author, columnist, and editor of DSP DesignLine has selected the very best digital signal processing design material from the Newnes portfolio and has compiled it into this volume. The result is a book covering the gamut of DSP design'from design fundamentals to optimized multimedia techniques'with a strong pragmatic emphasis. In addition to specific design techniques and practices, this book also discusses various approaches to solving DSP design problems and how to successfully apply theory to actual design tasks. The material has been selected for its timelessness as well as for its relevance to contemporary embedded design issues. CONTENTS: Chapter 1 ADCs, DACs, and Sampling Theory Chapter 2 Digital Filters Chapter 3 Frequency Domain Processing Chapter 4 Audio Coding Chapter 5 Video Processing Chapter 6 Modulation Chapter 7 DSP Hardware Options Chapter 8 DSP Processors and Fixed-Point Arithmetic Chapter 9 Code Optimization and Resource Partitioning Chapter 10 Testing and Debugging DSP Systems *Hand-picked content selected by Kenton Williston, Editor of DSP DesignLine *Proven best design practices for image, audio, and video processing *Case histories and design examples get you off and running on your current project

Euro-Par 2019: Parallel Processing Workshops - Ulrich Schwardmann 2020-05-29

This book constitutes revised selected papers from the workshops held at 25th International Conference on Parallel and Distributed Computing, Euro-Par 2019, which took place in Göttingen, Germany, in August 2019.

The 53 full papers and 10 poster papers presented in this volume were carefully reviewed and selected from 77 submissions. Euro-Par is an annual, international conference in Europe, covering all aspects of parallel and distributed processing. These range from theory to practice, from small to the largest parallel and distributed systems and infrastructures, from fundamental computational problems to full-edged applications, from architecture, compiler, language and interface design and implementation to tools, support infrastructures, and application performance aspects. Chapter "In Situ Visualization of Performance-Related Data in Parallel CFD Applications" is available open access under a Creative Commons Attribution 4.0 International License via link.springer.com.

Virtual Reality and Augmented Reality - Patrick Bourdot 2019-10-07

This book constitutes the refereed proceedings of the 16th International Conference on Virtual Reality and Augmented Reality, EuroVR 2019, held in Tallinn, Estonia, in October 2019. The 11 full papers and 5 short papers presented together with 8 scientific posters were carefully reviewed and selected from 54 submissions. The papers are organized in topical sections named: Immersive Interaction; Training, Teaching and Learning; Industrial Applications and Data Analysis; Perception, Cognition and Evaluation; and Scientific Posters.

Advanced Signal Integrity for High-Speed Digital Designs -

Stephen H. Hall 2011-09-20

A synergistic approach to signal integrity for high-speed digital design

This book is designed to provide contemporary readers with an understanding of the emerging high-speed signal integrity issues that are creating roadblocks in digital design. Written by the foremost experts on the subject, it leverages concepts and techniques from non-related fields such as applied physics and microwave engineering and applies them to high-speed digital design—creating the optimal combination between theory and practical applications. Following an introduction to the importance of signal integrity, chapter coverage includes: Electromagnetic fundamentals for signal integrity Transmission line fundamentals Crosstalk Non-ideal conductor models, including surface roughness and frequency-dependent inductance Frequency-dependent properties of dielectrics Differential signaling Mathematical requirements of physical channels S-parameters for digital engineers Non-ideal return paths and via resonance I/O circuits and models Equalization Modeling and budgeting of timing jitter and noise System analysis using response surface modeling Each chapter includes many figures and numerous examples to help readers relate the concepts to everyday design and concludes with problems for readers to test their understanding of the material. **Advanced Signal Integrity for High-Speed Digital Designs** issuitable as a textbook for graduate-level courses on signal integrity, for programs taught in industry for professional engineers, and as a reference for the high-speed digital designer.

Applied Reconfigurable Computing - Kentaro Sano 2015-03-30

This book constitutes the refereed proceedings of the 11th International Symposium on Applied Reconfigurable Computing, ARC 2015, held in Bochum, Germany, in April 2015. The 23 full papers and 20 short papers presented in this volume were carefully reviewed and selected from 85 submissions. They are organized in topical headings named: architecture and modeling; tools and compilers; systems and applications; network-on-a-chip; cryptography applications; extended abstracts of posters. In addition, the book contains invited papers on funded R&D - running and completed projects and Horizon 2020 funded projects.

Practical Problems in VLSI Physical Design Automation - Sung Kyu Lim 2008-07-31

Practical Problems in VLSI Physical Design Automation contains problems and solutions related to various well-known algorithms used in VLSI physical design automation. Dr. Lim believes that the best way to learn new algorithms is to walk through a small example by hand. This knowledge will greatly help understand, analyze, and improve some of the well-known algorithms. The author has designed and taught a graduate-level course on physical CAD for VLSI at Georgia Tech. Over the years he has written his homework with such a focus and has maintained typeset version of the solutions.

High-Speed Digital System Design - Anatoly Belous 2019-11-13

This book describes for readers the entire, interconnected complex of theoretical and practical aspects of designing and organizing the production of various electronic devices, the general and main distinguishing feature of which is the high speed of processing and transmitting of digital signals. The authors discuss all the main stages of design - from the upper system level of the hierarchy

(telecommunications system, 5G mobile communications) to the lower level of basic semiconductor elements, printed circuit boards. Since the developers of these devices in practice deal with distorted digital signals that are transmitted against a background of interference, the authors not only explain the physical nature of such effects, but also offer specific solutions as to how to avoid such parasitic effects, even at the design stage of high-speed devices.

High-level Synthesis - Michael Fingeroff 2010

Are you an RTL or system designer that is currently using, moving, or planning to move to an HLS design environment? Finally, a comprehensive guide for designing hardware using C++ is here. Michael Fingeroff's High-Level Synthesis Blue Book presents the most effective C++ synthesis coding style for achieving high quality RTL. Master a totally new design methodology for coding increasingly complex designs! This book provides a step-by-step approach to using C++ as a hardware design language, including an introduction to the basics of HLS using concepts familiar to RTL designers. Each chapter provides easy-to-understand C++ examples, along with hardware and timing diagrams where appropriate. The book progresses from simple concepts such as sequential logic design to more complicated topics such as memory architecture and hierarchical sub-system design. Later chapters bring together many of the earlier HLS design concepts through their application in simplified design examples. These examples illustrate the fundamental principles behind C++ hardware design, which will translate to much larger designs. Although this book focuses primarily on C and C++ to present the basics of C++ synthesis, all of the concepts are equally applicable to SystemC when describing the core algorithmic part of a design. On completion of this book, readers should be well on their way to becoming experts in high-level synthesis.

SpiNNaker - A Spiking Neural Network Architecture - Steve Furber 2020-03-15

This book tells the story of the origins of the world's largest neuromorphic computing platform, its development and its deployment, and the immense software development effort that has gone into making it openly available and accessible to researchers and students the world over

Applied Reconfigurable Computing. Architectures, Tools, and Applications - Nikolaos Voros 2018-04-25

This book constitutes the proceedings of the 14th International Conference on Applied Reconfigurable Computing, ARC 2018, held in Santorini, Greece, in May 2018. The 29 full papers and 22 short papers presented in this volume were carefully reviewed and selected from 78 submissions. In addition, the volume contains 9 contributions from research projects. The papers were organized in topical sections named: machine learning and neural networks; FPGA-based design and CGRA optimizations; applications and surveys; fault-tolerance, security and communication architectures; reconfigurable and adaptive architectures; design methods and fast prototyping; FPGA-based design and applications; and special session: research projects.

ASIC/SoC Functional Design Verification - Ashok B. Mehta 2017-06-28

This book describes in detail all required technologies and methodologies needed to create a comprehensive, functional design verification strategy and environment to tackle the toughest job of guaranteeing first-pass working silicon. The author first outlines all of the verification sub-fields at a high level, with just enough depth to allow an engineer to grasp the field before delving into its detail. He then describes in detail industry standard technologies such as UVM (Universal Verification Methodology), SVA (SystemVerilog Assertions), SFC (SystemVerilog Functional Coverage), CDV (Coverage Driven Verification), Low Power Verification (Unified Power Format UPF), AMS (Analog Mixed Signal) verification, Virtual Platform TLM2.0/ESL (Electronic System Level) methodology, Static Formal Verification, Logic Equivalency Check (LEC), Hardware Acceleration, Hardware Emulation, Hardware/Software Co-verification, Power Performance Area (PPA) analysis on a virtual platform, Reuse Methodology from Algorithm/ESL to RTL, and other overall methodologies.

A History of the Internet and the Digital Future - Johnny Ryan 2010-09-15

A History of the Internet and the Digital Future tells the story of the development of the Internet from the 1950s to the present and examines how the balance of power has shifted between the individual and the state in the areas of censorship, copyright infringement, intellectual freedom, and terrorism and warfare. Johnny Ryan explains how the Internet has revolutionized political campaigns; how the development of

the World Wide Web enfranchised a new online population of assertive, niche consumers; and how the dot-com bust taught smarter firms to capitalize on the power of digital artisans. From the government-controlled systems of the Cold War to today's move towards cloud computing, user-driven content, and the new global commons, this book reveals the trends that are shaping the businesses, politics, and media of the digital future.

SystemVerilog for Verification - Chris Spear 2012-02-14

Based on the highly successful second edition, this extended edition of SystemVerilog for Verification: A Guide to Learning the Testbench Language Features teaches all verification features of the SystemVerilog language, providing hundreds of examples to clearly explain the concepts and basic fundamentals. It contains materials for both the full-time verification engineer and the student learning this valuable skill. In the third edition, authors Chris Spear and Greg Tumbush start with how to verify a design, and then use that context to demonstrate the language features, including the advantages and disadvantages of different styles, allowing readers to choose between alternatives. This textbook contains end-of-chapter exercises designed to enhance students' understanding of the material. Other features of this revision include: New sections on static variables, print specifiers, and DPI from the 2009 IEEE language standard Descriptions of UVM features such as factories, the test registry, and the configuration database Expanded code samples and explanations Numerous samples that have been tested on the major SystemVerilog simulators SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Third Edition is suitable for use in a one-semester SystemVerilog course on SystemVerilog at the undergraduate or graduate level. Many of the improvements to this new edition were compiled through feedback provided from hundreds of readers.

Multi-Processor System-on-Chip 1 - Liliana Andrade 2021-03-12

A Multi-Processor System-on-Chip (MPSoC) is the key component for complex applications. These applications put huge pressure on memory, communication devices and computing units. This book, presented in two volumes - Architectures and Applications - therefore celebrates the 20th anniversary of MPSoC, an interdisciplinary forum that focuses on multi-core and multi-processor hardware and software systems. It is this interdisciplinarity which has led to MPSoC bringing together experts in these fields from around the world, over the last two decades. Multi-Processor System-on-Chip 1 covers the key components of MPSoC: processors, memory, interconnect and interfaces. It describes advance features of these components and technologies to build efficient MPSoC architectures. All the main components are detailed: use of memory and their technology, communication support and consistency, and specific processor architectures for general purposes or for dedicated applications.

FPGAs - Juan Jose Rodriguez Andina 2017-07-28

Field Programmable Gate Arrays (FPGAs) are currently recognized as the most suitable platform for the implementation of complex digital systems targeting an increasing number of industrial electronics applications. They cover a huge variety of application areas, such as: aerospace, food industry, art, industrial automation, automotive, biomedicine, process control, military, logistics, power electronics, chemistry, sensor networks, robotics, ultrasound, security, and artificial vision. This book first presents the basic architectures of the devices to familiarize the reader with the fundamentals of FPGAs before identifying and discussing new resources that extend the ability of the devices to solve problems in new application domains. Design methodologies are discussed and application examples are included for some of these domains, e.g., mechatronics, robotics, and power systems.

FPGAs for Software Programmers - Dirk Koch 2016-06-17

This book makes powerful Field Programmable Gate Array (FPGA) and reconfigurable technology accessible to software engineers by covering different state-of-the-art high-level synthesis approaches (e.g., OpenCL and several C-to-gates compilers). It introduces FPGA technology, its programming model, and how various applications can be implemented on FPGAs without going through low-level hardware design phases. Readers will get a realistic sense for problems that are suited for FPGAs and how to implement them from a software designer's point of view. The authors demonstrate that FPGAs and their programming model reflect the needs of stream processing problems much better than traditional CPU or GPU architectures, making them well-suited for a wide variety of systems, from embedded systems performing sensor processing to large setups for Big Data number crunching. This book serves as an invaluable tool for software designers and FPGA design

engineers who are interested in high design productivity through behavioural synthesis, domain-specific compilation, and FPGA overlays. Introduces FPGA technology to software developers by giving an overview of FPGA programming models and design tools, as well as various application examples; Provides a holistic analysis of the topic and enables developers to tackle the architectural needs for Big Data processing with FPGAs; Explains the reasons for the energy efficiency and performance benefits of FPGA processing; Provides a user-oriented approach and a sense for where and how to apply FPGA technology.

Low Power Methodology Manual - David Flynn 2007-07-31

This book provides a practical guide for engineers doing low power System-on-Chip (SoC) designs. It covers various aspects of low power design from architectural issues and design techniques to circuit design of power gating switches. In addition to providing a theoretical basis for these techniques, the book addresses the practical issues of implementing them in today's designs with today's tools.

Distributed Computing and Artificial Intelligence, 17th International Conference - Yucheng Dong 2020-08-06

This book brings together past experience, current work and promising future trends associated with distributed computing, artificial intelligence and their application in order to provide efficient solutions to real problems. DCAI 2020 is a forum to present applications of innovative techniques for studying and solving complex problems in artificial intelligence and computing areas. This year's technical program will present both high quality and diversity, with contributions in well-established and evolving areas of research. Specifically, 83 papers were submitted to main track and special sessions, by authors from 26 different countries representing a truly "wide area network" of research activity. The DCAI'20 technical program has selected 35 papers and, as in past editions, it will be special issues in ranked journals. This symposium is organized by the University of L'Aquila (Italy). We would like to thank all the contributing authors, the members of the Program Committee and the sponsors (IBM, Armundia Group, EurAI, AEPIA, APPIA, CINI, OIT, UGR, HU, SCU, USAL, AIR Institute and UNIVAQ).

Brain Storm Optimization Algorithms - Shi Cheng 2019-06-03

Brain Storm Optimization (BSO) algorithms are a new kind of swarm intelligence method, which is based on the collective behavior of human beings, i.e., on the brainstorming process. Since the introduction of BSO algorithms in 2011, many studies on them have been conducted. They not only offer an optimization method, but could also be viewed as a framework of optimization techniques. The process employed in the algorithms could be simplified as a framework with two basic operations: the converging operation and the diverging operation. A "good enough" optimum could be obtained through recursive solution divergence and convergence. The resulting optimization algorithm would naturally have the capability of both convergence and divergence. This book is primarily intended for researchers, engineers, and graduate students with an interest in BSO algorithms and their applications. The chapters cover various aspects of BSO algorithms, and collectively provide broad insights into what these algorithms have to offer. The book is ideally suited as a graduate-level textbook, whereby students may be tasked with the study of the rich variants of BSO algorithms that involves a hands-on implementation to demonstrate the utility and applicability of BSO algorithms in solving optimization problems.

Efficient Processing of Deep Neural Networks - Vivienne Sze 2020-06-24

This book provides a structured treatment of the key principles and techniques for enabling efficient processing of deep neural networks (DNNs). DNNs are currently widely used for many artificial intelligence (AI) applications, including computer vision, speech recognition, and robotics. While DNNs deliver state-of-the-art accuracy on many AI tasks, it comes at the cost of high computational complexity. Therefore, techniques that enable efficient processing of deep neural networks to improve metrics—such as energy-efficiency, throughput, and latency—without sacrificing accuracy or increasing hardware costs are critical to enabling the wide deployment of DNNs in AI systems. The book includes background on DNN processing; a description and taxonomy of hardware architectural approaches for designing DNN accelerators; key metrics for evaluating and comparing different designs; features of the DNN processing that are amenable to hardware/algorithm co-design to improve energy efficiency and throughput; and opportunities for applying new technologies. Readers will find a structured introduction to the field as well as a formalization and organization of key concepts from contemporary works that provides insights that may spark new ideas.

Memory Controllers for Mixed-Time-Criticality Systems - Sven Goossens

2016-04-11

This book discusses the design and performance analysis of SDRAM controllers that cater to both real-time and best-effort applications, i.e. mixed-time-criticality memory controllers. The authors describe the state of the art, and then focus on an architecture template for reconfigurable memory controllers that addresses effectively the quickly evolving set of SDRAM standards, in terms of worst-case timing and power analysis, as well as implementation. A prototype implementation of the controller in SystemC and synthesizable VHDL for an FPGA development board are used as a proof of concept of the architecture template.

Data Plane Development Kit (DPDK) - Heqing Zhu 2020-11-19

This book brings together the insights and practical experience of some of the most experienced Data Plane Development Kit (DPDK) technical experts, detailing the trend of DPDK, data packet processing, hardware acceleration, packet processing and virtualization, as well as the practical application of DPDK in the fields of SDN, NFV, and network storage. The book also devotes many chunks to exploring various core software algorithms, the advanced optimization methods adopted in DPDK, detailed practical experience, and the guides on how to use DPDK.

Advanced HDL Synthesis and SOC Prototyping - Vaibhav Taraate 2018-12-15

This book describes RTL design using Verilog, synthesis and timing closure for System On Chip (SOC) design blocks. It covers the complex RTL design scenarios and challenges for SOC designs and provides practical information on performance improvements in SOC, as well as Application Specific Integrated Circuit (ASIC) designs. Prototyping using modern high density Field Programmable Gate Arrays (FPGAs) is discussed in this book with the practical examples and case studies. The book discusses SOC design, performance improvement techniques, testing and system level verification, while also describing the modern Intel FPGA/XILINX FPGA architectures and their use in SOC prototyping. Further, the book covers the Synopsys Design Compiler (DC) and Prime Time (PT) commands, and how they can be used to optimize complex ASIC/SOC designs. The contents of this book will be useful to students and professionals alike.

Getting Started with Raspberry Pi 3 - Agus Kurniawan 2016-03-05

Raspberry Pi 3 model B is a new Raspberry Pi board which included WiFi and Bluetooth modules. This book helps you to get started with Raspberry Pi 3. The following is highlight topics in this book: *

Introduction to Raspberry Pi 3 * Operating System * Powering Up and Running * Connecting to a Network : Wired and WiFi * Raspberry Pi Programming * Working with Bluetooth and iBeacon * Deploying LAMP Stack * Accessing GPIO * Raspberry Pi 3 Serial Debugging

EDA for IC Implementation, Circuit Design, and Process Technology - Luciano Lavagno 2018-10-03

Presenting a comprehensive overview of the design automation algorithms, tools, and methodologies used to design integrated circuits, the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes. The second volume, EDA for IC Implementation, Circuit Design, and Process Technology, thoroughly examines real-time logic to GDSII (a file format used to transfer data of semiconductor physical layout), analog/mixed signal design, physical verification, and technology CAD (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale, power supply network design and analysis, design modeling, and much more. Save on the complete set.

PCB Design for Real-World EMI Control - Bruce R. Archambeault 2013-06-29

Proper design of printed circuit boards can make the difference between a product passing emissions requirements during the first cycle or not. Traditional EMC design practices have been simply rule-based, that is, a list of rules-of-thumb are presented to the board designers to implement. When a particular rule-of-thumb is difficult to implement, it is often ignored. After the product is built, it will often fail emission requirements and various time consuming and costly add-ons are then required. Proper EMC design does not require advanced degrees from universities, nor does it require strenuous mathematics. It does require a basic understanding of the underlying principles of the potential causes of EMC emissions. With this basic understanding, circuit board designers can make trade-off decisions during the design phase to ensure optimum EMC design. Consideration of these potential sources will allow the design to pass the emissions requirements the first time in the test laboratory. A number of other books have been published on EMC. Most are general books on EMC and do not focus on printed circuit board is

intended to help EMC engineers and design design. This book engineers understand the potential sources of emissions and how to reduce, control, or eliminate these sources. This book is intended to be a 'hands-on' book, that is, designers should be able to apply the concepts in this book directly to their designs in the real-world.

Right the First Time - Lee W. Ritchey 2003

High Performance Computing - Michela Taufer 2016-10-05

This book constitutes revised selected papers from 7 workshops that were held in conjunction with the ISC High Performance 2016 conference in Frankfurt, Germany, in June 2016. The 45 papers presented in this volume were carefully reviewed and selected for inclusion in this book. They stem from the following workshops: Workshop on Exascale Multi/Many Core Computing Systems, E-MuCoCoS; Second International Workshop on Communication Architectures at Extreme Scale, ExaComm; HPC I/O in the Data Center Workshop, HPC-IODC; International Workshop on OpenPOWER for HPC, IWOPH; Workshop on the Application Performance on Intel Xeon Phi - Being Prepared for KNL and Beyond, IXPUG; Workshop on Performance and Scalability of Storage Systems, WOPSSS; and International Workshop on Performance Portable Programming Models for Accelerators, P3MA.

Signal and Power Integrity--simplified - Eric Bogatin 2010

With the inclusion of the two new hot topics in signal integrity, power integrity and high speed serial links, this book will be the most up to date complete guide to understanding and designing for signal integrity.

Real-Time Embedded Systems - Christos Koulamas 2019-01-10

This book is a printed edition of the Special Issue "Real-Time Embedded Systems" that was published in Electronics

Prototypical - Don Dinger 2016-05-21

The first half of "PROTOTYPICAL" is a concise history of FPGA-based prototyping. We go back to the beginning, briefly introducing the debut of the Altera EP300 in 1984 and the Xilinx XC2064 in 1985. We then discuss the tipping point for what would become FPGA-based prototyping: the introduction of the Quickturn Systems RPM in May 1988. Strictly speaking, the RPM was an FPGA-based hardware emulator, but it set the stage for a radical change in chip development methodology. Intel took the Quickturn technology and put the P5 microarchitecture through its paces on a 14-machine cluster, running a killer demo in 1991 and ultimately releasing the Pentium microprocessor in 1993. From there, while the large EDA firms scuffled over bigger and bigger hardware emulation capability, several academic teams started deploying FPGAs for reconfigurable computing and rapid prototyping. These teams were looking for lower cost ways to prove out algorithms and chip designs. It was during this period issues of FPGA interconnect and synthesis partitioning were uncovered and addressed - and just in time, as ARM7TDMI synthesizable cores appeared in 1997. We then launch into chapters with brief timelines of three of the major firms in FPGA-based prototyping: S2C, Synopsys, and Cadence. We close the first half with a look at where FPGA-based prototyping is headed, including how it can help application segments such as automotive, wearables, and the IoT - three segments we believe will see an increasing number of design starts as new players seek to optimize and differentiate their software through chip design. The second half of "PROTOTYPICAL" is an all-new Field Guide titled "Implementing an FPGA Prototyping Methodology" authored by the teams at S2C. It looks at when design teams need an FPGA-based prototyping solution, how to choose one, and how to be sure the platform is scalable including a look at the latest cloud-based implementations. It then dives into the methodology: setting up a prototype, partitioning, interconnect, debugging, and exercising a design. It's a practical view of the questions teams have and the issues they run into, and how to solve them.

Benchmarking, Measuring, and Optimizing - Wanling Gao 2020-06-09

This book constitutes the refereed proceedings of the Second International Symposium on Benchmarking, Measuring, and Optimization, Bench 2019, held in Denver, CO, USA, in November 2019. The 20 full papers and 11 short papers presented were carefully reviewed and selected from 79 submissions. The papers are organized in topical sections named: Best Paper Session; AI Challenges on Cambircon using AIBenc; AI Challenges on RISC-V using AIBench; AI Challenges on X86 using AIBench; AI Challenges on 3D Face Recognition using AIBench; Benchmark; AI and Edge; Big Data; Datacenter; Performance Analysis; Scientific Computing.

Processor and System-on-Chip Simulation - Rainer Leupers 2010-09-15

Simulation of computer architectures has made rapid progress recently. The primary application areas are hardware/software performance estimation and optimization as well as functional and timing verification. Recent, innovative technologies such as retargetable simulator generation, dynamic binary translation, or sampling simulation have enabled widespread use of processor and system-on-chip (SoC) simulation tools in the semiconductor and embedded system industries. Simultaneously, processor and SoC simulation is still a very active research area, e.g. what amounts to higher simulation speed, flexibility, and accuracy/speed trade-offs. This book presents and discusses the principle technologies and state-of-the-art in high-level hardware architecture simulation, both at the processor and the system-on-chip level.

Semiconductor Circuit Design - Bryan Norris 1975

Spin Current - Sadamichi Maekawa 2012-07-26

Since the discovery of the giant magnetoresistance (GMR) effect in magnetic multilayers in 1988, a new branch of physics and technology, called spin-electronics or spintronics, has emerged, where the flow of electrical charge as well as the flow of electron spin, the so-called "spin current", are manipulated and controlled together. Recent progress in the physics of magnetism and the application of spin current has progressed in tandem with the nanofabrication technology of magnets and the engineering of interfaces and thin films. This book is intended to provide an introduction and guide to the new physics and applications of spin current. The emphasis is placed on the interaction between spin and charge currents in magnetic nanostructures.